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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/667,046	09/21/2000	Steven A. Lytle	LYTLE 18	8375

7590 05/29/2002
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EXAMINER

VU, HUNG K

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 05/29/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/667,046

Applicant(s)

LYTLE, STEVEN A.

Examiner

Hung K. Vu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 March 2002.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 21-28 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 21-28 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the transistors, as recited in claim 25; a third dielectric layer and a landing pad, as recited in claim 27; and the via that extends through the third dielectric, as recited in claim 28, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 22 and 27 are objected to because of the following informalities: In claim 22, line 3, and claim 27, lines 2 and 3, after "second" insert --interlevel-- for clarity. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

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(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 21 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Bandyopadhyay et al. (PN 5,827,776). Note Figures 1 – 13 of Bandyopadhyay et al.. Bandyopadhyay et al. discloses a semiconductor device comprising,

a first metal feature (12) located over a semiconductor surface (20) and having a first interlevel dielectric layer (22) located thereover and a second interlevel dielectric layer (24) located over the first interlevel dielectric layer, the second interlevel dielectric layer having a second metal feature (26) located in a surface thereof;

an unsegmented via (38) located through the first and second interlevel dielectric layers, the via extending between and connecting the first metal feature and the second metal feature, the via being void of a landing pad between the first and second interlevel dielectric layers.

With regard to claims 24, Bandyopadhyay et al. discloses the via is a passing metal via with no passing metal feature.

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4. Claims 21-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoo et al. (PN 6,177,340). Note Figures 1-20 of Yoo et al..

Yoo et al. discloses a semiconductor device comprising,

a first metal feature (9) located over a semiconductor surface (1) and having a first interlevel dielectric layer (19) located thereover and a second interlevel dielectric layer (23) located over the first interlevel dielectric layer, the second interlevel dielectric layer having a second metal feature (31) located in a surface thereof;

an unsegmented via (27,28) located through the first and second interlevel dielectric layers, the via extending between and connecting the first metal feature and the second metal feature, the via being void of a landing pad between the first and second interlevel dielectric layers.

With regard to claims 22, Yoo et al. discloses the via is a first via and the semiconductor device further includes a second via (21,29) located through the first and second dielectric layers and wherein a trench structure (25) is located over and connects with the second via.

With regard to claims 23, Yoo et al. discloses the device further including a trench structure located adjacent the via.

With regard to claims 24, Yoo et al. discloses the via is a passing metal via with no passing metal feature.

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With regard to claims 25, Yoo et al. discloses the device further including transistors (10) wherein the first metal feature is located over the transistors and interconnect the transistors to form an operative integrated circuit.

With regard to claims 26, Yoo discloses the device further including a damascene structure located adjacent the via.

5. Claims 21-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang (PN 6,127,260). Note Figures 1-20 of Huang.

Huang discloses a semiconductor device comprising,

a first metal feature (8) located over a semiconductor surface (1) and having a first interlevel dielectric layer (20) located thereover and a second interlevel dielectric layer (31) located over the first interlevel dielectric layer, the second interlevel dielectric layer having a second metal feature (44) located in a surface thereof;

an unsegmented via (42a) located through the first and second interlevel dielectric layers, the via extending between and connecting the first metal feature and the second metal feature, the via being void of a landing pad between the first and second interlevel dielectric layers.

With regard to claims 22, Huang discloses the via is a first via and the semiconductor device further includes a second via (41a) located through the first and second interlevel dielectric layers and wherein a trench structure is located over and connects with the second via.

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With regard to claims 23, Huang discloses the device further including a trench structure located adjacent the via.

With regard to claims 24, Huang discloses the via is a passing metal via with no passing metal feature.

With regard to claims 25, Huang discloses the device further including transistors (10) wherein the first metal feature is located over the transistors and interconnect the transistors to form an operative integrated circuit.

With regard to claims 26, Huang discloses the device further including a damascene structure located adjacent the via.

With regard to claims 27, Huang discloses the device further including a third dielectric layer (48) located over the second interlevel dielectric layer and a landing pad located between the second interlevel dielectric layer and the third dielectric layer.

With regard to claims 28, Huang discloses the device further including a via (47,48) that extends through the third dielectric layer and contacts the landing pad.

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Response to Arguments

6. Applicant's arguments with respect to claim 21 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (703) 308-4079. The examiner can normally be reached on Mon-Thurs 7:00-5:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the

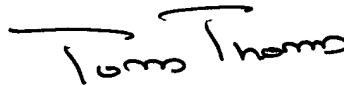
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organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

May 25, 2002


TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800